IN THE CLAIMS:

Please amend the claims as follows.

1-20 (Cancelled)

21. (Currently Amended) A computer system comprising:

a plurality of processing sets, each having at least one processor, and

a bridge coupled to each of said processing sets and operable to monitor a step locked operation of said processing sets,

wherein each of said processors comprises a processor identification register ~~which is~~comprising:

a first field which is read/writeable and which is configured to store ~~in said register~~ data representative of a processor version of the processor; and

a second field which is configured to store data representative of a configuration of the processor, ~~representative of a processor identification,~~

wherein each of said processors being configured, consequent upon a predetermined condition, to load a common predefined data value that is common to said processing sets into said first field of its processor identification register.

22. (Previously presented) A computer system as claimed in Claim 21, wherein said predetermined condition is a reset state of at least one of said plurality of processors.

23. (Previously presented) A computer system as claimed in Claim 22, wherein said reset state is a state asserted in said computer system following boot or re-boot.

24. (Previously presented) A computer system as claimed in Claim 21, wherein each of said processing sets includes a boot memory unit storing data which is representative of initialization code arranged to initialize said processor to operate within said computer system, said boot memory unit including said common predefined data value which is loaded by said processor into said processor identification register.

25. (Previously presented) A computer system as claimed in Claim 24, wherein said boot memory unit is a programmable read-only memory.

26. (Previously presented) A computer system as claimed Claim 21, wherein said common predefined data value is an all zeros value.

27. (Previously presented) A computer system as claimed in Claim 21, wherein each of said processors further includes a read only register having stored therein said processor identification data.

28. (Previously presented) A computer system as claimed in Claim 27, wherein said processor identification data stored in said read only register is loaded, upon initialization into said processor identification register.

29. (Previously presented) A computer system as claimed in Claim 21, wherein said common predefined value is a processor identification of one of the processors of said computer system, said processor identification of each of said processors being matched.

30. (Currently Amended) A processor for use in a processing set forming part of a fault tolerant computer system that ~~includes~~ comprises a plurality of processing sets, said processor comprising:

an interface for communication with an I/O bus, and

a processor identification register coupled to said interface, said register comprises:

a first field which is read/writeable and which is configured to store data representative of a processor version of the processor; and

a second field which is configured to store data representative of a configuration of the processor~~identification~~,

wherein said processor is responsive to a masking condition, to write a common predefined data value received via said I/O bus into said first field of said processor

identification register, wherein said predefined data value is common to said processing sets and is operable to mask said data representative of a processor ~~identification~~version.

31. (Previously presented) A processor as claimed in Claim 30, comprising a read only register having stored therein said processor identification data, wherein said processor identification data stored in said read only register is loadable, upon initialization into said processor identification register.

32. (Currently Amended) A method of operating a fault tolerant computer system comprising a plurality of processing sets, each of ~~which~~ said processing sets is connected to a bridge, each of said processing sets having at least one processor, wherein at least a first processor in said computer system comprising a processor identification register comprising:

a first field which is read/writeable and which is configured to store data representative of a processor version of the processor; and

a second field which is configured to store data representative of a configuration of the processor,

said method comprising ~~the steps of~~:

detecting a predetermined condition representative of a state in which a processor identification is present in the processor identification register of said first processor; and

loading a common predefined data value into said first field of processor identification register of said first processor, which predefined data value is common to said processing sets and is operable to mask said processor ~~identification~~version.

33. (Previously presented) A method of operating a fault tolerant computer system as claimed in Claim 32, wherein said predetermined condition is a reset state of at least a processing set comprising said first processor.

34. (Previously presented) A method of operating a fault tolerant computer system as claimed in Claim 33, wherein said reset state is a state asserted in said fault tolerant computer

system following boot or re-boot.

35. (Previously presented) A method of operating a fault tolerant computer system as claimed in Claim 32, comprising:

detecting an error condition of at least a processing set comprising said first processor, and

if said error condition is detected performing the step of loading said common predefined data value in said processor identification register of said first processor.

36. (Currently Amended) A method of operating a fault tolerant computer system comprising a plurality of processing sets, each having at least one processor, and a bridge coupled to each of said processing sets and operable to monitor a step locked operation of said processing sets, said method comprising ~~the steps of~~:

removing a processor of one of said processing sets; and

replacing the removed processor with a replacement processor that ~~includes~~ comprises:

an interface for communication with an I/O bus, and

a processor identification register comprising:

a first field which is read/writeable and which has ~~stored in said register~~ data representative of a processor ~~identification~~version of the processor stored therein; and

a second field which has data representative of a configuration of the processor stored therein,

wherein said replacement processor is responsive to a masking condition, to write a common predefined data value received via said I/O bus into said first field of said processor identification register, wherein said predefined data value is common to said processing sets and is operable to mask data representative of a said processor ~~identification~~version.

37. (Previously presented) A method of operating a fault tolerant computer system as claimed

in Claim 36, wherein said replacement processor is replaced by replacing one of said processing sets with a processing set having the replacement processor.